Application Note

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Document No.: AN1111

APM32F103xB Hardware Development Guide

Version: V1.0

1 Introduction

This application note is a minimum design specification for system hardware of the APM32F103xB series, including power supply scheme, clock source, reset mode, startup mode settings, and debugging management.

The detailed reference design drawing is also included in this document, including descriptions of main components, interfaces, and modes.

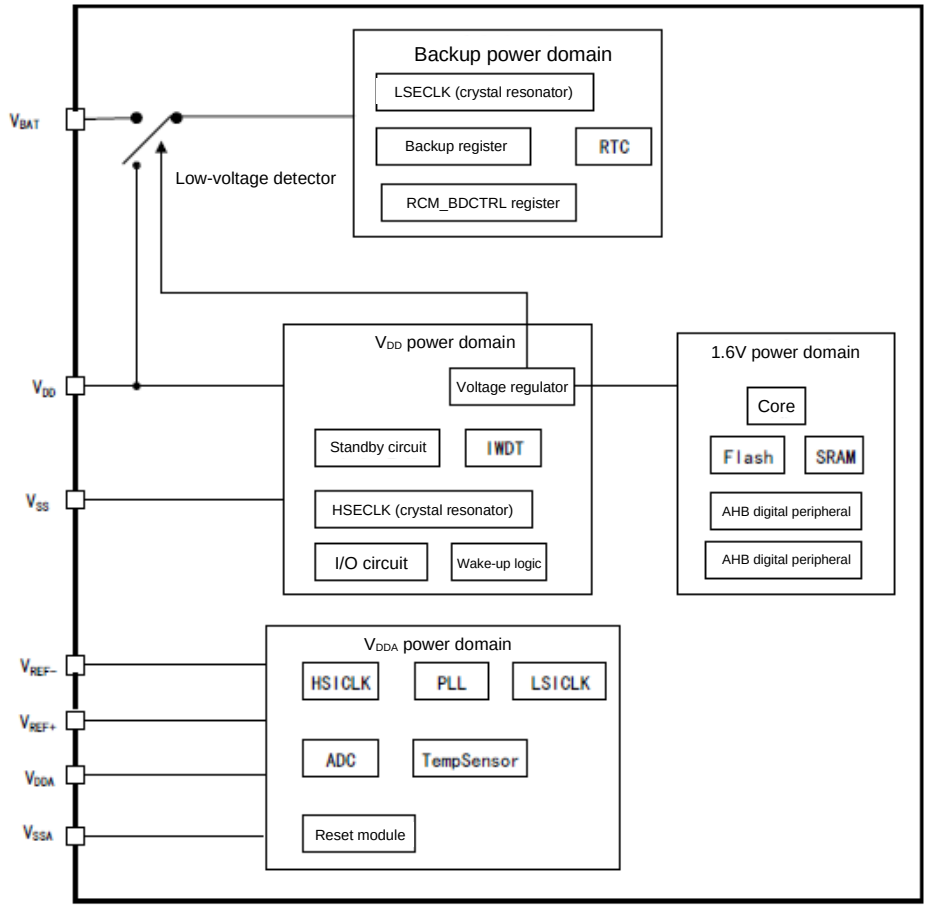
Contents

2 Power supply

2.1 Introduction

The power supply is the basis for stable operation of a system. The operating voltage is 2.0~3.6V. It can provide 1.6V power supply through the built-in voltage regulator. If the main power VDD is powered down, it can supply power to the backup power supply area through VBAT.

Figure 1Power Supply Control Structure Block Diagram



2.1.1 Voltage regulator

Power can be supplied to 1.6V power domain in the following operating modes:

- Normal mode: In this mode, 1.6V power supply area runs at full power
- Stop mode: In this mode, 1.6V power supply area works in low-power state, all clocks are off, and peripherals stop work
- Standby mode: In this mode, 1.6V power supply area stops power supply, and except for the standby circuit, the content of register and SRAM will be lost.

2.1.2 Backup power field

- When VDD exists, the backup power supply area is powered by VDD. When VDD is powered down, the backup power supply area is powered by VBAT, which is used to save the content of backup register and maintain RTC function. Suppply power to LSECLK crystal resonator, RTC, backup register, RCM_BDCTRL register, PC13, PC14, and PC15.
- V_{BAT} must be connected to V_{DD} externally when no external battery is used.

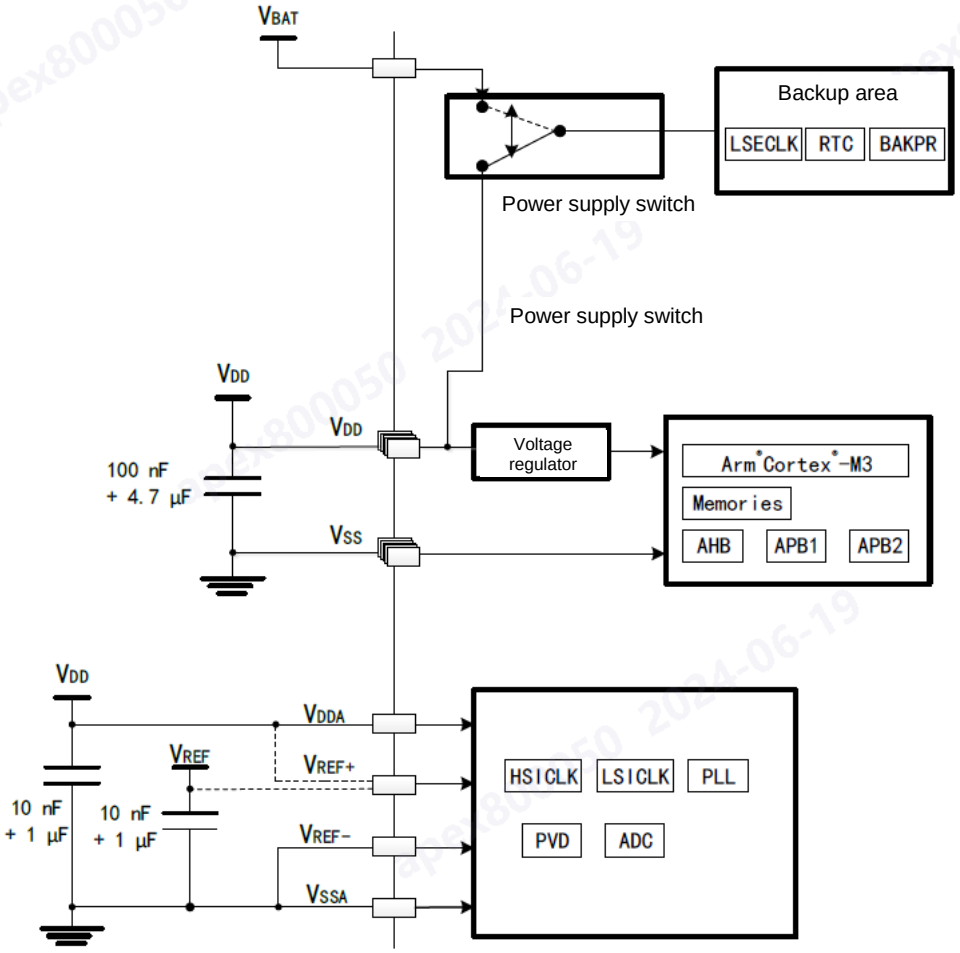
2.1.3 Independent ADC power supply and reference voltage

Independent ADC power supply can improve the conversion accuracy, and the specific power pins are as follows:

- V_{DDA}: Power pin of ADC
- V_{SSA}: Independent power ground pin
- V_{REF+} /V_{REF-}: Reference voltage pin of ADC

2.2 Power Supply Scheme

Figure 2 Power Supply Scheme



Pay attention to the power supply range of each power domain:

Table 1 Power Supply Scheme

Name	Voltage range	Description
V_{DD}	2.0 ~ 3.6V	VDD powers IO interface directly, and powers the core circuit through the voltage regulator.
V_{DDA}	2.4 ~ 3.6V	Connected to VDD to power the analog part of ADC, reset module, RC oscillator, and PLL. When ADC is used, VDDA is greater than or equal to 2.4V. VDDA and VSSA must be connected to VDD and VSS respectively.
V_{BAT}	1.8V~3.6V	When VDD is turned off, it automatically powers the RTC, external 32.768KHz oscillator, and backup register.

Where:

Table 2 Precautions for Power Domain

V_{DD}	V_{DD} must be connected to V_{DD} power supply of an external capacitor (X 100nF ceramic capacitor(s) (1) and a tantalum capacitor not less than 4.7μF). V_{DDX} represents that the number of V_{DD} is x.
V_{BAT}	The V_{BAT} pin can be connected to an external battery (1.8V<3.6V). If there is no external battery, an external 100nF ceramic capacitor (1) is required to be connected to the V_{DD} power supply together.
V_{DDA}	The V_{DDA} pin must be connected to an external capacitor (10nF ceramic capacitor (1) + 1μF tantalum capacitor).
V_{REF+}	The V_{REF+} pin can be directly connected to V_{DDA} or separately use an external reference voltage. A 10nF and a 1μF ceramic capacitor (1) must be connected to this pin. Meanwhile, the voltage range of V_{REF+} must be between 2.4V and V_{DDA}.

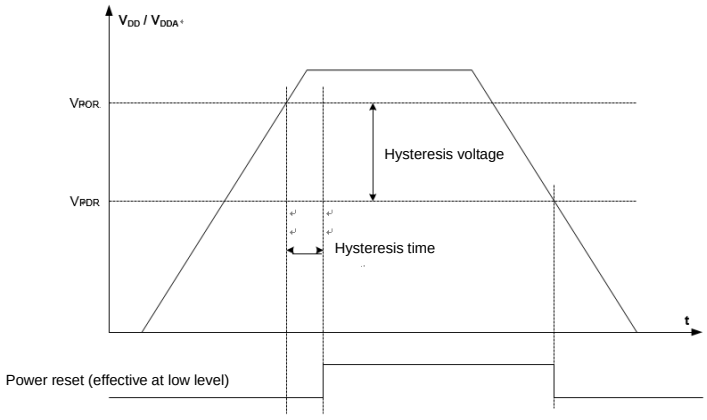
(1) It is recommended to use the ceramic capacitors made of X7R

2.3 Power Management and Reset

2.3.1 Power-on reset and power-down reset (POR and PDR)

When the VDD/VDDA is lower than the threshold voltage VPOR and VPDR , the chip will automatically remain in the reset state. The waveform diagrams of power-on reset and power-down reset are as follows. For POR, PDR, hysteresis voltage and hysteresis time, please refer to the Datasheet.

Figure 3 Power-on Reset and Power-down Reset Oscillogram



2.3.2 Power Voltage Detector (PVD)

A threshold can be set for PVD to monitor whether VDD /VDDA is higher or lower than the threshold. If the interrupt is enabled, the interrupt can be triggered to process the VDD/VDDA exceeding the threshold in advance. The usage of PVD is as follows:

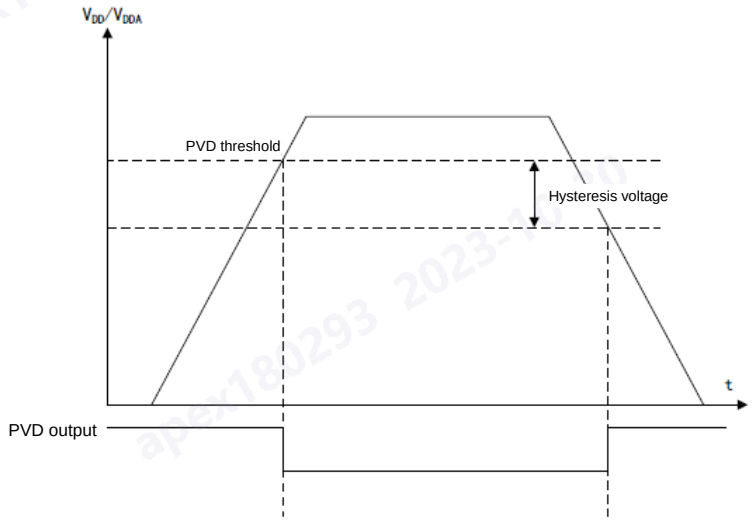
(1) Set the PVDEN bit of the configuration register PMU_CTRL to 1 to enable PVD

(2) Select the voltage threshold of PVD through the PLSEL[2:0] bit of the configuration register PMU_CTRL

(3) The PVDOFLG bit of the configuration register PMU_CSTS indicates whether the value of VDD is higher or lower than the threshold of PVD

(4) When VDD/VDDA is detected to be below or above the PVD threshold, a PVD interrupt will be generated, and the threshold waveform is shown below. Please see the *Datasheet* for PVD threshold and hysteresis voltage.

Figure 4 PVD Threshold Oscillogram



2.3.3 System reset

The reset source is divided into external reset source and internal reset source.

Table 3 Reset Source

External reset source:	Low level on NRST pin.
Internal reset source:	(1) Window watchdog termination count (WWDT reset) (2) Independent watchdog termination count (IWDT reset) (3) Software reset (SW reset) (4) Low-power management reset (5) Power reset

A system reset will occur when any of the above events occurs. Besides, the reset event source can be identified by viewing the reset flag bit in RCM_CSTS (control/status register).

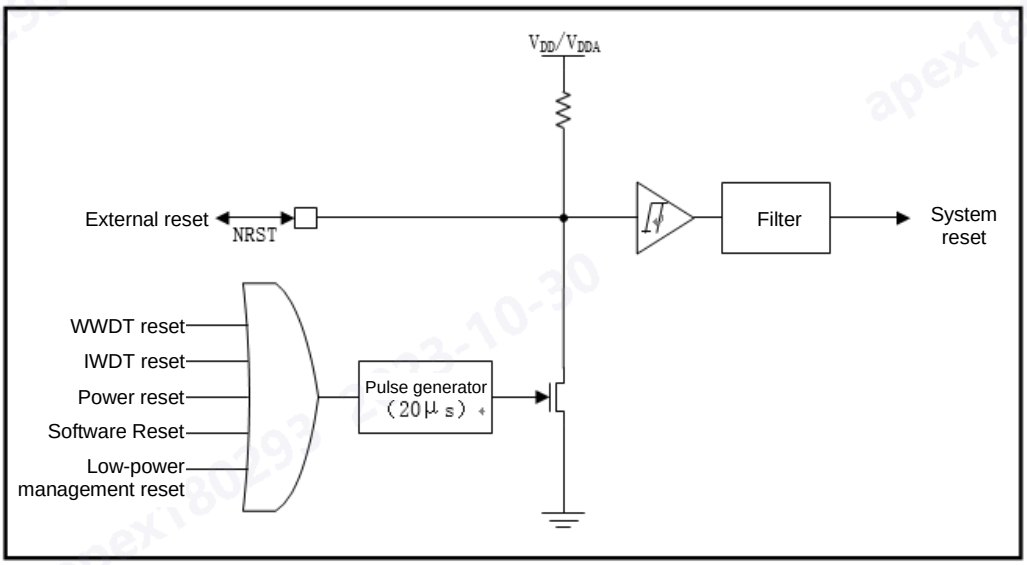
2.3.2.1 System reset circuit

The reset source is used in the NRST pin, which remains low in reset process. The internal reset source generates a pulse with a delay of at least 20μs on the NRST pin through the

pulse generator, which causes the NRST to maintain the level and generate reset; the external reset source directly pulls down the NRST pin level to generate reset.

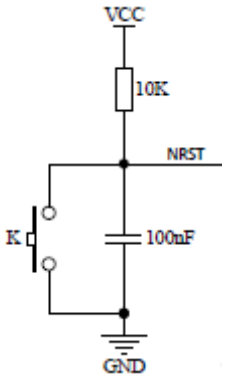
The system reset circuit is shown in Figure 5:

Figure 5 System Reset Circuit



Recommend external reset circuit

Figure 6 External Reset Circuit

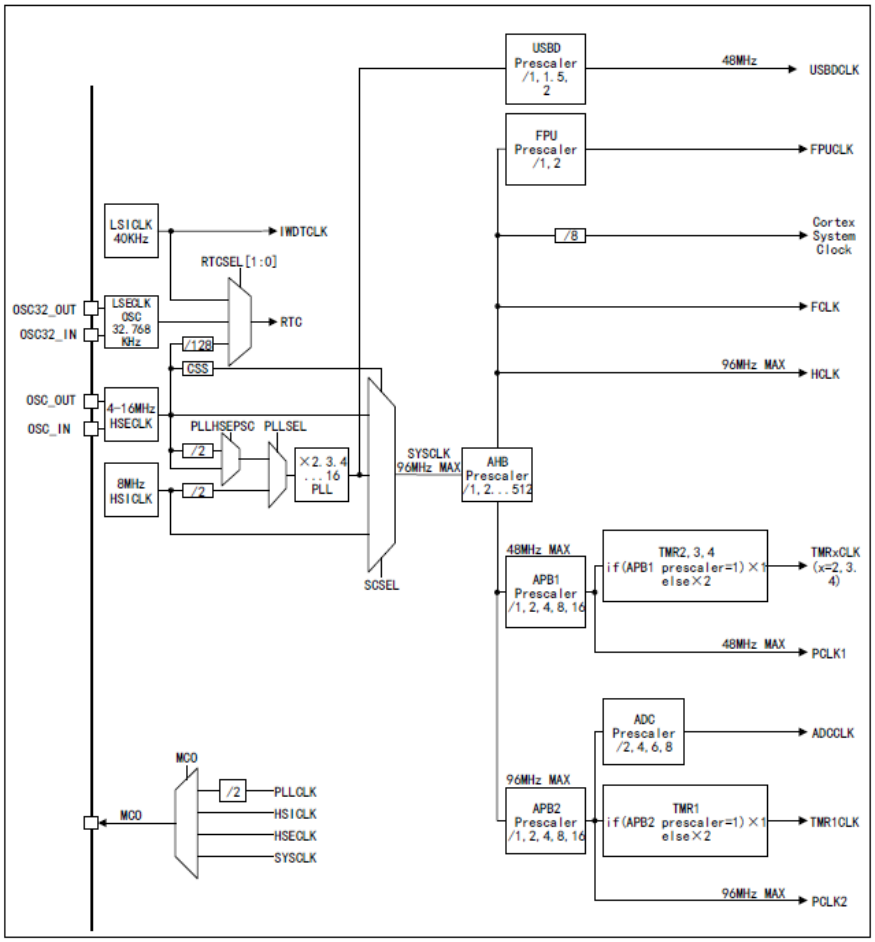


3 Clock

The clock sources of the whole system are: HSECLK, LSECLK, HSICLK, LSICLK and PLL. For the characteristics of the clock source, please refer to the relevant chapter of "Electrical Characteristics" in the datasheet.

Clock tree:

Figure 7 Clock Tree



3.1 External clock source

The external clock signal includes HSECLK (high-speed external clock signal) and LSECLK (low-speed external clock signal).

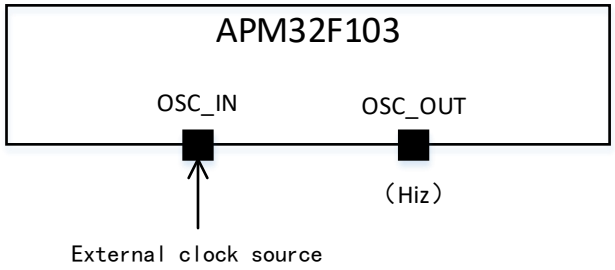
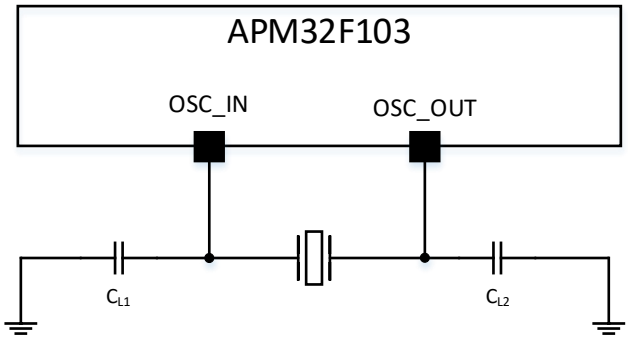
There are two kinds of external clock sources:

- External clock of user
- External crystal/ceramic resonator

The hardware configuration of the two kinds of clock sources is shown in the figure below.

Figure 4 HSECLK/LSECLK Clock Source Hardware Configuration

Clock source	Hardware configuration

External clock	
Crystal/Ceramic resonator	

(1) In order to reduce the distortion of clock output and shorten the startup stabilization time, the crystal/ceramic resonator and load capacitor must be as close to the oscillator pin as possible. The value of the matching capacitance (C_{L1}, C_{L2}) must be adjusted according to the selected oscillator.

(2) The load capacitor C_L follows the formula of: $C_L=C_{L1}$ x C_{L2} / ($C_{L1}+C_{L2}$) + C_S. C_S is relevant capacitance of PCB and MCU pins. The typical value is between 2pF and 10pF.

3.1.1 HSECLK high-speed external clock signal

HSECLK clock signal is generated by two kinds of clock sources, i.e. HSECLK external crystal/ceramic resonator and HSECLK external clock .

Table 5 Clock Source Generating HSECLK

Name	Description
External clock source (HSECLK bypass)	Provide clock to the MCU through OSC_IN pin. The signal can be generated by ordinary function signal transmitter (in debugging), crystal oscillator and other signal generators; the waveform can be square wave, sine wave or triangle wave with 50% duty cycle, and the maximum frequency is up to 25MHz. In hardware connection, it must be connected to the OSC_IN pin and the OSC_OUT pin must be suspended.
Name	Description
External crystal/ceramic resonator (HSECLK crystal)	The clock is provided to MCU by the resonator, and the resonator includes crystal resonator and ceramic resonator. The frequency range is 4-16MHz. OSC_IN, OSC_OUT is required to connect the resonator,

	and it can be turned on and off by setting the HSEEN bit in RCM_CTRL in the clock control register. Regarding the size of the external matching capacitor, please refer to the formula: $C_{L1}= C_{L2} = 2*(C_L- C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, and the typical value is 10pF. When selecting an external high-speed crystal resonator, it is recommended to select the one with a load capacitance of around 20pF, so that the external matching capacitors (1) C_{L1} and C_{L2} only need to have a capacitance value of 20pF, and the PCB should be as close as possible to the crystal oscillator pins.

(1) It is recommended to use the temperature compensation capacitors made of NPO (COG) for the matching capacitor of the crystal oscillator.

3.1.2 LSECLK low-speed external clock signal

LSECLK clock signal is generated by two kinds of clock sources, i.e. LSECLK external crystal/ceramic resonator and LSECLK external clock .

Table 6 Clock Source Generating LSECLK

Name	Description
External clock source (LSECLK bypass)	The clock is provided to MCU by OSC32_IN pin. The signal can be generated by ordinary function signal transmitter (in debugging), crystal oscillator and other signal generators; the waveform can be square wave, sine wave or triangle wave with 50% duty cycle, and the signal frequency needs to be 32.768kHz. For hardware connection, it must be connected to OSC32_IN pin, ensuring OSC32_OUT pin is suspended; for MCU configuration, the user can select this mode by setting LSEBCFG and LSEEN bits in RCM_BDCTRL (backup domain control register).
External crystal/ceramic resonator (LSECLK crystal)	The clock is provided to MCU by the resonator, and the resonator includes crystal resonator and ceramic resonator. The frequency is 32.768kHz. When needing to connect OSC32_IN and OSC32_OUT to the resonator, it can be turned on and off through the LSEEN bit in RCM_BDCTRL. Regarding the size of the external matching capacitor, please refer to the formula: $C_{L1}= C_{L2} = 2*(C_L - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, and the typical value is 5pF. When selecting an external crystal resonator, it is recommended to select the one with a load capacitance of around 10pF, so that the external matching capacitors (1) C_{L1} and C_{L2} only need to have a capacitance value of 10pF, and the PCB should be as close as possible to the crystal

	oscillator pins during layout.

(1) It is recommended to use the temperature compensation capacitors made of NPO or COG for the matching capacitor of the crystal oscillator.

4 Startup configuration

Since the CPU of Arm® Cortex®-M3 core obtains the reset vector from the ICode Bus (instruction bus), the startup can only start from the code area, and the typical one is Flash memory startup. However, APM32 MCU series realizes a special mechanism. By configuring the BOOT[1:0] pin parameter, there are three different startup modes, and the system can not only start from Flash memory or system memory, but also start from the built-in SRAM. The memory selected as the start zone is determined by the selected startup mode.

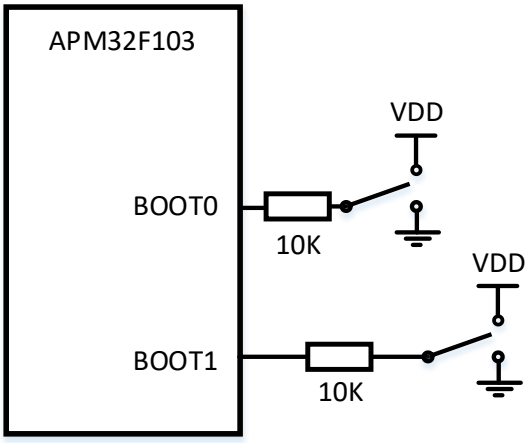
Table 7Startup Mode Configuration and Access Mode

Startup mode selection pin		Startup mode	Access methods
BOOT0	BOOT1		
0	X	Main flash memory (Flash)	The main flash memory is mapped to the boot space, but it can still be accessed at its original address, that is, the contents of the flash memory can be accessed in two address areas.
1	0	System memory	The system memory is mapped to the boot space (0x00000000), but it can still be accessed at its original address.
1	1	Built-in SRAM	SRAM can be accessed only at the starting address.

- The user can select the startup mode after reset by setting the states of BOOT1 and BOOT0 pins.
- BOOT pin should keep the startup configuration required by user in standby mode. When exiting the standby mode, the value of boot pin will be latched.
- If you choose to start from built-in SRAM, you must use NVIC's exception table and offset register to remap the vector table to SRAM when writing the application code.

Recommended BOOT circuit design:

Figure 8 Recommended BOOT Circuit Design



5 Debugging interface (SWJ-DP)

The product supports serial debugging interface (SW-DP) and JTAG (JTAG-DP) debugging interface.

Table 8 Debugging Interface

SW-DP	SW-DP interface provides 2-pin (data + clock) interface for AHB module. Among them, some of 2 pins of SW-DP interface and 5 pins of JTAG interface are multiplexed.
JTAG	JTAG interface provides 5-pin standard JTAG interface for AHB access port.

5.1 Debugging Pin Function Configuration

- Realize the on-line programming and debugging of the chip.
- Use KEIL/IAR and other software to implement on-line debugging, downloading and programming.
- Flexible implementation of production of bus-off programmer.

Table 9 Pin Function Configuration

SWJ- CFG[2:0]	Configured as dedicated pin for debugging	I/O port assignment of SWJ interface				
		PA13/ JTMS/ SWDIO	PA14/ JTCK/ SWCLK	PA15/ JTDI	PB3/ JTDO	PB4/ JNTRST
Others	Disable	Release				
100	Both JTAG-DP interface and SW-DP interface are disabled					

	Disable					
010	JTAG-DP interface is disabled, and SW-DP interface is enabled	Special	Special	Release		
001	All SWJ pins (JTAG-DP+SW-DP) Except JNTRST pin	Special	Special	Special	Special	Release
000	All SWJ pins (JTAG-DP+SW-DP) Reset state	Special	Special	Special	Special	Special

5.2 IO status during reset and just after reset

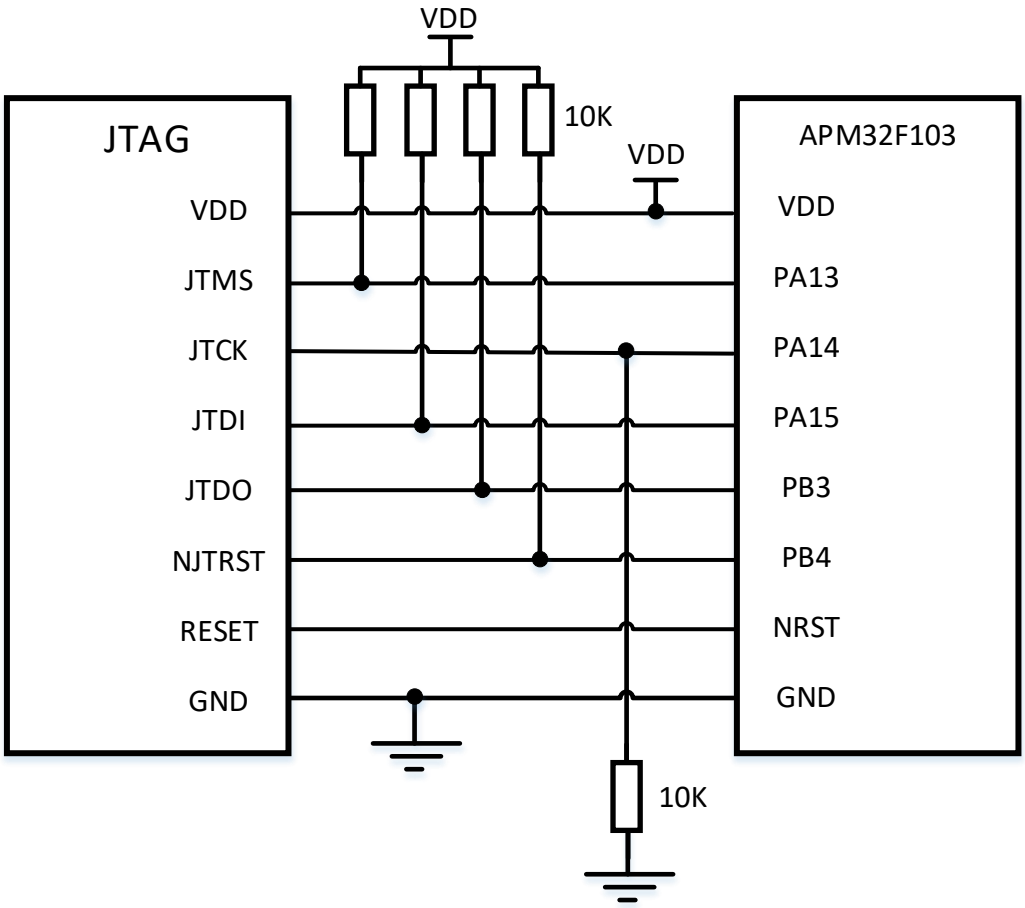
If the multiplexing function is not enabled during and just after GPIO reset, the I/O port will be configured as floating input mode, and in such case, the pull-up/pull-down resistor is disabled in input mode. After reset, the JTAG pin is put in the input pull-up or pull-down mode, and the specific configuration is as follows:

- PA15: JTDI is set to pull-up mode;
- PA14: JTCK is set to pull-down mode;
- PA13: JTMS in pull-up mode
- PB4: JNTRST is set to pull-up mode;
- PB3: JTDO is in floating mode.

5.3 Recommended Debugging Interface Circuit

Recommended JTAG interface reference design:

Figure 9 JTAG Interface Circuit

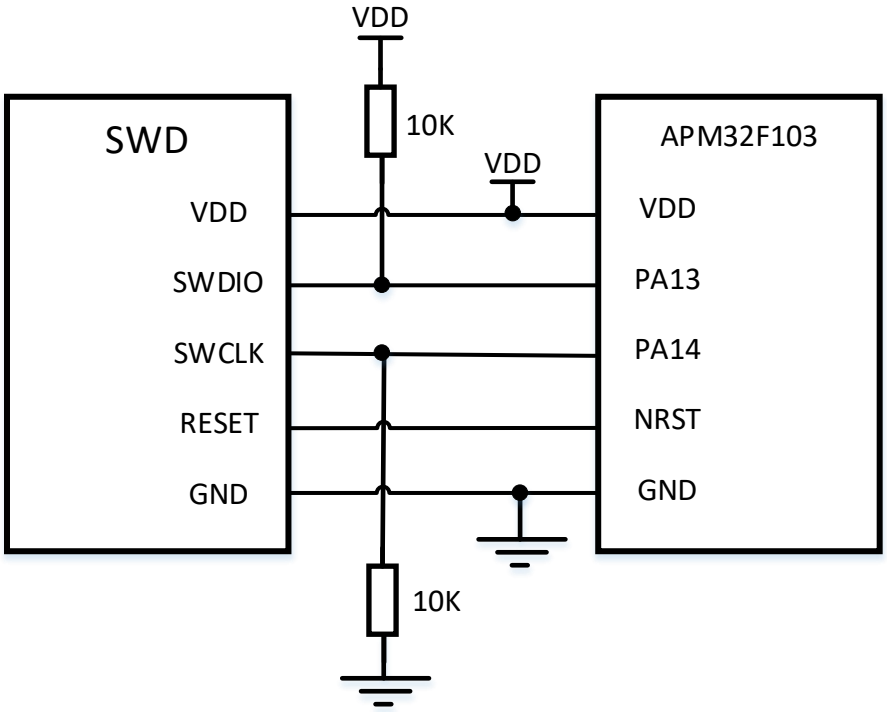


Note:

(1) The JTAG interface reference design is to add an external pull-up resistor to the JTMS, JTDI, JTDO, and NJTRST pins, and add a pull-down resistor to the JTCK pin, which can enhance the anti-interference capability of downloading and debugging. If these pins are multiplexed for other functions, please evaluate the impact of pull-up and pull-down resistors and make adjustments based on the actual situation.

Recommended SWD interface reference design:

Figure 10 SWD Interface Circuit



Note:

(1) The reference design for the SWD interface is to add an external pull-up resistor and pull-down resistor to the SWDIO and SWCLK pins, which can enhance the anti-interference ability of downloading and debugging. If these two pins are multiplexed for other functions, please evaluate the impact of the pull-up and pull-down resistors and make adjustments according to the actual situation.

6 Design Suggestions

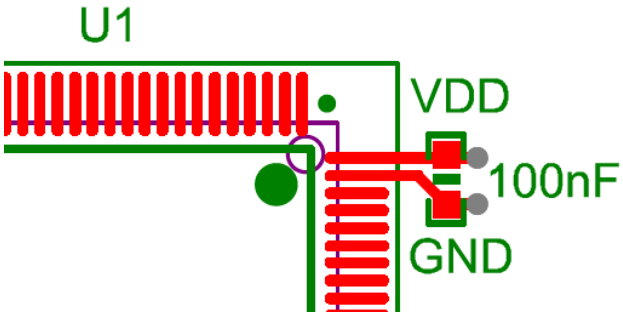
6.1 PCB Stacking

- Number of layers: It is recommended to use the multi-layer design to ensure independent GND and power layers, which can better ensure signal integrity and enhance shielding effect. However, considering the costs, users can reduce the number of stacking layers while ensuring good grounding and power supply.
- Signal and formation: The signal layer should be adjacent to the formation. This helps to reduce the electromagnetic interference and the loop area of the signal path, and can serve as a reference plane for the signal.
- Power supply and formation: The power supply layer should be separated from the formation.

6.2 Power Supply Design

- Stable power input: Ensure stable power supply and filter the power noise.
- Decoupling capacitors: Place one or more 100nF decoupling capacitors at each VDD pin near the chip.

Figure 11 Recommended Power Pin Decoupling Capacitor Layout Design



- Power supply wiring: It is recommended that the power supply wiring should be wide and short enough to reduce the influence of parasitic parameters and the voltage drop.

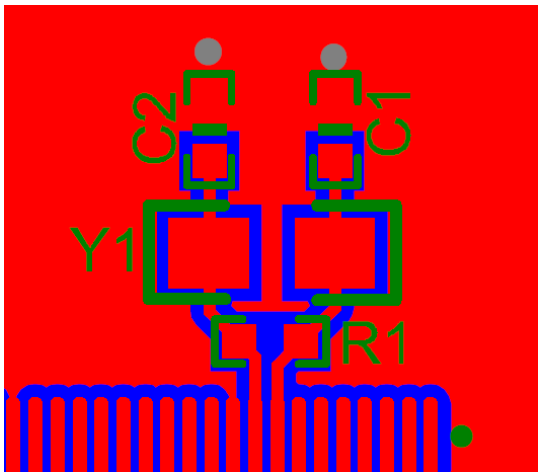
6.3 Clock Design

- Crystal oscillator selection: Choose an appropriate crystal oscillator and ensure it meets the operating frequency and stability requirements of the MCU.
- Wiring suggestions: Clock signal wiring should be as short as possible and be away from strong interference signals such as high current and high-speed signal

lines. It is recommended to use package processing to enhance the shielding effect.

- Layout suggestions: The crystal oscillator circuit should be placed close to the chip, and to reduce the interference, it is best to ensure a complete ground plane below the entire crystal oscillator circuit.

Figure 12 Recommended Clock Pin Layout Design



6.4 I/O Design

- I/O configuration: Correctly configure the modes of I/O ports, such as input, output, pull-up and pull-down, and open-drain mode.
- Protection: For externally connected I/O ports, consider adding the voltage protection (TVS tube) and series resistor.

6.5 EMC and EMI

- Layout: Consider the design of electromagnetic compatibility (EMC) and electromagnetic interference (EMI), and the layout should be reasonable. For example, keep the MCU away from high-power and strong interference sources, and consider how to reduce the loop area, etc.
- Shielding: Use shielding and reasonable grounding strategies for sensitive and high-speed circuits.

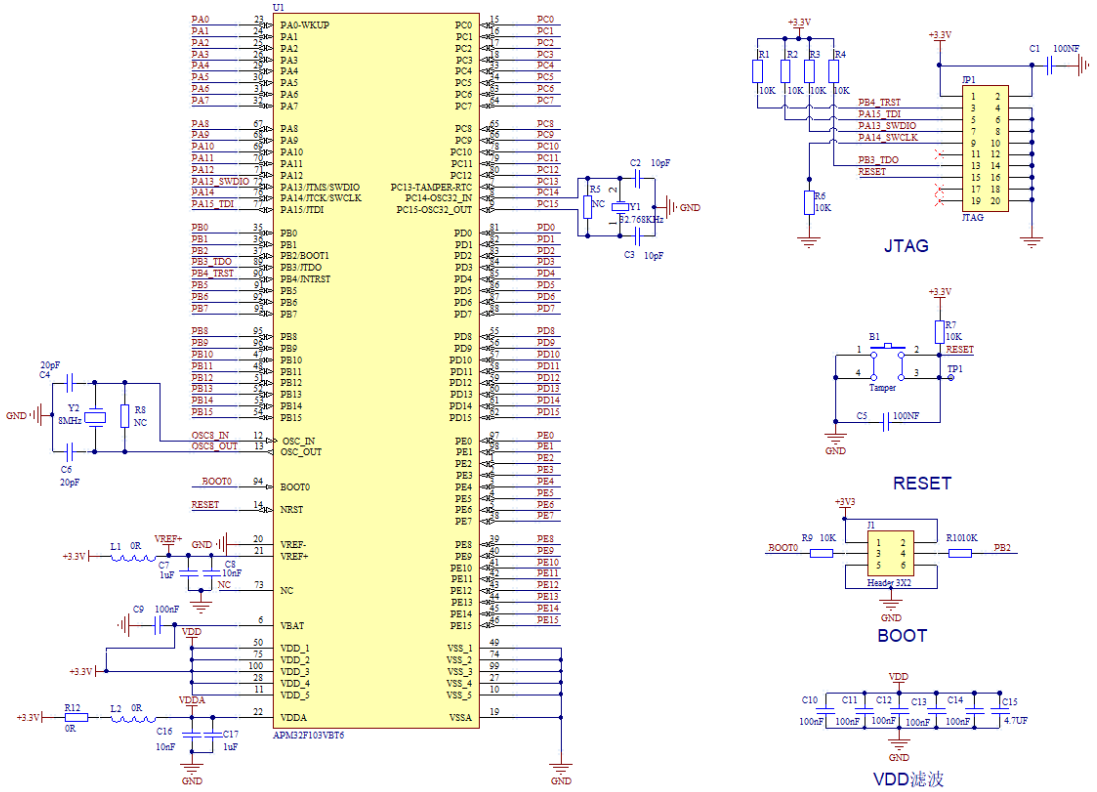
6.6 Grounding

- Single-point grounding: In low-frequency circuits or circuits with not high noise requirements, adopting single-point grounding can avoid formation of ground loop. In such case, all grounding points should be connected to a common grounding point, which is usually the negative pole of the power supply or some grounding plane on the circuit board.

- Multi-point grounding: In high-frequency circuits or high-current circuits, usually multi-point grounding is used. The grounding of each component or function module is directly connected to the nearest grounding plane, which can reduce the impedance of the ground wire, and reduce the noise and electromagnetic interference.
- Separation of analog from digital ground: If the MCU processes the analog and digital signals simultaneously, the analog ground and digital ground should be processed separately. This can be achieved by physically separating two ground planes and merging them at a certain point to connect them to the main ground, which can reduce the interference of digital noise with the analog signals.

6.7 Reference Schematic Diagram Design

Figure 13 Reference Schematic Diagram



7 Revision history

Table 10 Document Revision History

Date	Version	Revision History
June, 2024	V1.0	New edition

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8. Scope of Application

The information in this document replaces the information provided in all previous versions of the document.